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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/475,262	12/30/1999	BEN D. ROBERTS	042390.P6809	6144

7590 04/09/2003

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EXAMINER

CRAIG, DWIN M

ART UNIT	PAPER NUMBER
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2123

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DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No

09/475,262

Applicant(s)

ROBERTS, BEN D. *ppe*

Examiner

Dwin M Craig

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 December 1999.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-63 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-63 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 December 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other: _____

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DETAILED ACTION

1. Claims 1-63 have been presented for examination. Claims 1-63 have been examined and rejected.

Claim Objections

2. **Claim 17** is objected to because of the following informalities: in line 3 at the end of the sentence there is the phrase “resistors is series” this phrase should be changed to “resistors in series”. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 1-3, 5-13, 15-20, 22-35, 37-45, 47-52 and 54-63** are rejected under 35 U.S.C. as being unpatentable over **Nakamura U.S. Patent 6,192,330** in view of **Muddu U.S. Patent 6,314,546** and in further view of **Dannsky et al. U.S. Patent 6,028,989**.

3.1 As regards independent **Claims 1, 18, 28, 29, 33, 50 and 60** the *Nakamura* reference discloses, a machine readable storage medium with at least one processor (**Figure 35 Item 6, Col. 7 Lines 39-50**), and a string model (**Figures 3, 5, 6, 9, 22A, 22B, 23, 24, 25, 26, 27, 28, 30A, 30B, 30C, 34**).

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However, the *Nakamura* reference does not expressly disclose modeling a trace lumped elements, cross capacitors, a pi model and applied noise voltage.

The *Muddu* reference discloses modeling a trace (**Figure 1**), a pi model (**Figures 8b, 8c**).

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because (*motivation to combine*) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, (*Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50*).

The *Nakamura* reference does not expressly disclose lumped elements, cross capacitors and applied noise voltage.

The *Dannsky et al.* reference discloses lumped elements (**Col. 7 Lines 9-67, Col. 8 Lines 1-6**) cross capacitors (**Col. 7 Line 16**), and applied noise voltage (**Col. 1 Lines 15-18, Lines 63-67, Col. 2 Lines 1-17**).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because (*motivation to combine*) it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design (*Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33*).

3.2 As regards the limitation disclosed in independent **Claim 28** regarding an apparatus, the *Nakamura* reference discloses (**Figure 35**).

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3.3 As regards **Claims 2, 3, 5, 19, 20, 22, 23, 34, 35, 37, 51, 52 and 54** the *Nakamura* does not expressly disclose reducing the number of capacitors and resistors in the model and the O'Brien/Savarino method.

The *Muddu* reference discloses reducing the number of capacitors and resistors in the model and the O'Brien/Savarino method, (**Figure 4, Col. 5 Lines 35-67, Col. 6 Lines 1-67, Col. 7 Lines 1-2**).

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because (*motivation to combine*) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, (*Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50*).

3.4 As regards **Claims 6, 38 and 55** the *Nakamura* reference does not expressly disclose a "pi" model.

The *Muddu* reference discloses a "pi" model (**Figure 8b and 8c**).

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because (*motivation to combine*) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, (*Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50*).

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3.5 As regards **Claims 7, 32, 39, 56 and 63** the *Nakamura* reference does not expressly disclose a voltage ramp.

The *Muddu* reference discloses a voltage ramp (**Figure 2b**).

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because (*motivation to combine*) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, (*Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50*).

3.6 As regards **Claims 8, 24 and 40** the *Nakamura* reference does not expressly disclose a ramp time and a driving transistor.

The *Muddu* reference discloses a ramp time and a driving transistor (**Figures 1, 2a, 2b, 3, 4, 5a, 5b, 6a, 6b, 7a, 7b, 8a, 8b, 8c, 8d and 8e, Col. 3 Lines 44-67, Col. 4 Lines 1-67, Col. 5 Lines 1-67, Col. 6 Lines 1-67, Col. 7 Lines 1-2**).

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because (*motivation to combine*) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, (*Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50*).

3.7 As regards **Claims 9 and 41** the *Nakamura* reference does disclose a string model, however it does not expressly disclose a pi model.

The *Muddu* reference discloses a pi model (**Figures 8b, 8c**).

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because (*motivation to combine*) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, (*Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50*).

3.8 As regards **Claims 10 and 42** the *Nakamura* reference does not expressly disclose a linear source.

The *Muddu* reference discloses a linear source model (**Figures 8a, 8c, Col. 8 Lines 8-14**).

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because (*motivation to combine*) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, (*Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50*).

3.9 As regards **Claims 11, 12, 43, 44 and 57** the *Nakamura* reference does not expressly disclose a victim node of the pi model.

The *Dansky et al.* reference discloses a victim node of the pi model (**Col. 1 Lines 24-26, Col. 3 Lines 15-16, Col. 3 Lines 40-48**).

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It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because (*motivation to combine*) it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design (*Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33*).

3.10 As regards **Claims 13, 26, 27, 58 and 59** the *Nakamura* reference does not expressly disclose a second noise voltage to the pi model.

The *Dansky et al.* reference discloses a second noise voltage applied to the pi model (**Col. 3 Lines 40-49**).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because (*motivation to combine*) it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design (*Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33*).

3.11 As regards **Claims 15, 16 and 25** the *Nakamura* reference does not expressly disclose calculating the peak noise.

The *Dansky et al.* reference discloses calculating peak noise (**Col. 7 Lines 60-67, Col. 8 Lines 1-6**).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because (*motivation to combine*) it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design (*Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33*).

3.12 As regards **Claims 17 and 49** the *Nakamura* reference does not expressly disclose resistors in series and capacitors in parallel reduced into a pi-model.

The *Muddu* reference discloses resistors in series (**Figure 5a, 5b, Col. 6 Lines 15-25**) and capacitors in parallel (**Figures 8b, 8c**).

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because (*motivation to combine*) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, (*Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50*).

3.13 As regards **Claims 30 and 61** the *Nakamura* reference does not expressly disclose discrete samples.

The *Muddu* reference discloses discrete load capacitances (**Col. 4 Lines 14-22**).

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because (*motivation to combine*) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, (*Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50*).

3.14 As regards **Claims 31, 45, 47, 48 and 62** the *Nakamura* reference does not expressly disclose applied noise voltage.

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The *Dannsky et al.* reference discloses applied noise voltage (**Col. 1 Lines 15-18, Lines 63-67, Col. 2 Lines 1-17**).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because (*motivation to combine*) it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design (*Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33*).

4. Claims 4, 21, 36 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nakamura U.S. Patent 6,192,330** in view of **Muddu U.S. Patent 6,314,546** and in further view of **Dannsky et al. U.S. Patent 6,028,989** and in further view of **“Modeling the Driving-Point Characteristics of Resistive Interconnect for Accurate Delay Estimation”, Peter R. O’Brien and Thomas L. Savarino, IEEE 1989** hereafter referred as the **O’Brien and Savarino** reference.

4.1 As regards independent **Claims 1, 18, 33, 50** see the rejection in paragraph 3.1.

4.2 As regards dependent **Claims 2, 3, 19, 20, 34, 35, 51 and 52** see the rejection in paragraph 3.3.

4.3 As regards **Claims 4, 21, 36, 53** the *Nakamura* reference does not expressly disclose the Elmore influence reduction method.

The *O’Brien and Savarino* reference discloses the Elmore influence reduction method (**pages 513-514**).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *O’Brien and Savarino* reference

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because (*motivation to combine*) the methods disclosed in the *O'Brien and Savarino* reference provides greater accuracy in determining the voltage transfer ration between gates in an integrated circuit, (*Abstact, Page 512 "Modeling the Driving-Point Characteristics of Resistive Interconnect for Accurate Delay Estimation", Peter R. O'Brien and Thomas L. Savarino, IEEE 1989*).

5. **Claims 14 and 46** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nakamura U.S. Patent 6,192,330** in view of **Muddu U.S. Patent 6,314,546** and in further view of **Dannsky et al. U.S. Patent 6,028,989** and in further view of **Arsenault et al. U.S. Patent 6,396,256**.

5.1 As regards independent **Claims 1 and 33** see the rejection in paragraph 3.1.

5.2 As regards dependent **Claims 13 and 45** see the rejection in paragraph 3.10 and 3.14 respectively.

5.5 As regards **Claims 14 and 46** the *Nakamura* reference does not expressly disclose voltage ramps having their ramp times in phase.

The *Arsenault et al.* reference discloses voltage ramps having their ramp times in phase (**Figures 2 and 3, Col. 1 Lines 45-55, Col. 2 Lines 48-63**).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Arsenault et al.* reference because (*motivation to combine*) the *Arsenault et al.* reference discloses a method of detecting defects in a design before manufacturing and therefore remove the requirement to have to redesign a product after the initial investment in manufacturing has been made, (*Arsenault et al. Col. 1 Lines 34-45*).

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Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
April 2, 2003


RUSSELL FREJD
PRIMARY EXAMINER